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Project Proposal – Impact of Supply Voltage Biasing

10/17/13

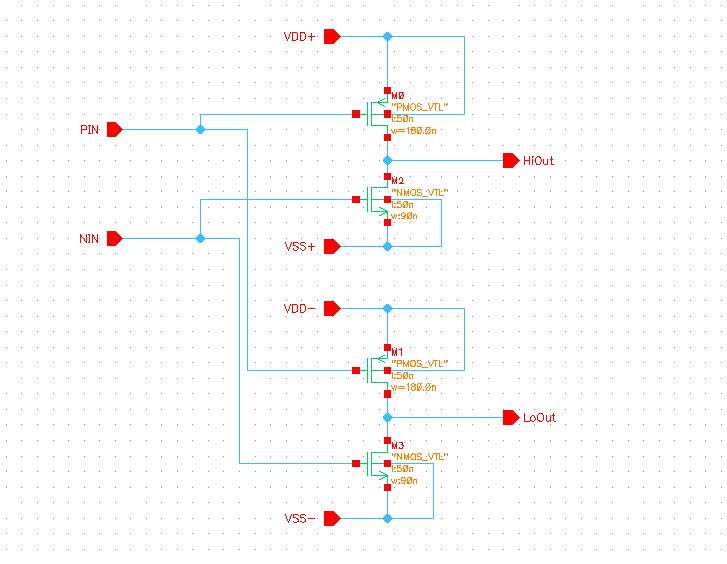
**Problem and Approach**

FinFETs are quite effective in improving FET power consumption and frequency. However, with continued scaling of integrated circuits (ICs), improvements in FET technology remain a crucial part of modern research. We, therefore, seek to explore methods for yet further improving power consumption and frequency in FinFETs. Body biasing is an effective method for influencing frequency and power consumption in traditional MOSFETs. Tschanz, *et al.* discuss this further in [1] and [2]. Because FinFETs are not significantly susceptible to body effects [3], alternate methods for influencing frequency and power consumption are necessary. Specifically, in this project, we will determine the impact of the source voltage on CMOS body biasing. We will do this by adjusting the source voltages for, first, a simple two-inverter setup and then ring oscillators of different sizes. It is important to note that our ring oscillators are constructed using two inverters for each gate rather than one. In a single two-inverter setup, we bias the top inverter with a +Vbias and the bottom inverter with a –Vbias. This is the design within each inverter in the ring oscillators as well.

In order for both group members to better understand this project and the results from simulations, it is important that each member participate, at least in some part, in each step of the project. It will be the responsibility of each team member to design, run, and evaluate simulations that have been discussed within the group. It is important to integrate the ideas of both members into simulations and designs in order to encourage a broader and deeper understanding of the results obtained.

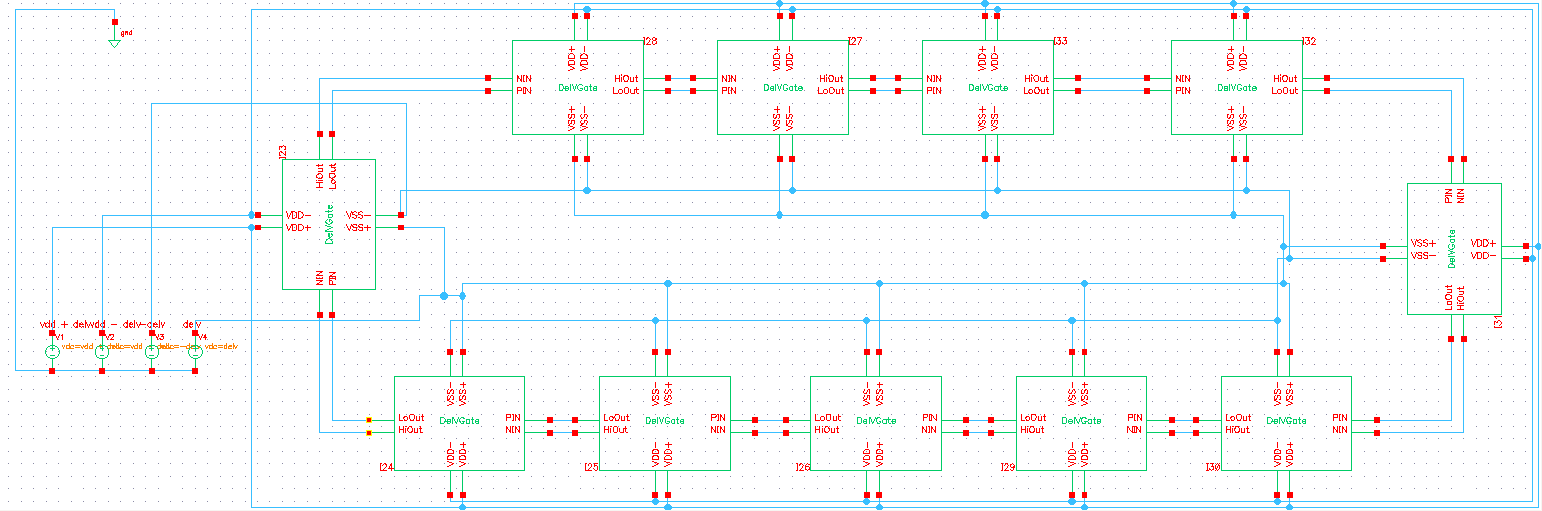
**Design**

In order to evaluate a change in frequency and/or power with varying supply voltages, the gate for the new design must include two inverters: one which will have its supply voltages shifted up by some bias voltage, and one which will have its supply voltages shifted down.Figure 1 illustrates this proposed design.



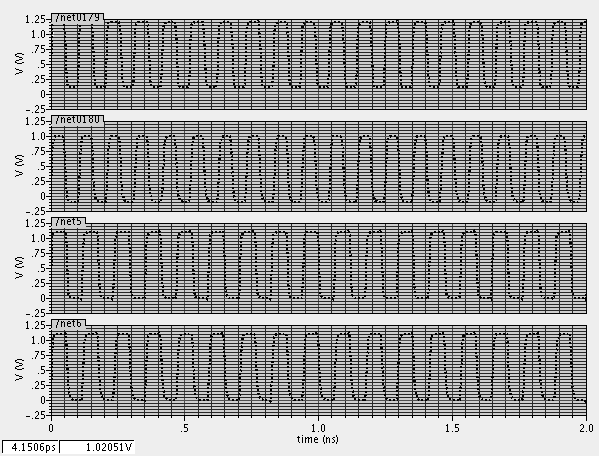
**Figure 1: Two-Inverter Gate with Variable Supply Voltages**

The transistors in this schematic have been minimally sized. The gate in Figure 1 has the same logical effort as a standard (one PMOS and one NMOS) inverter with transistors whose widths are twice those shown here. Notice that there are two inputs and two outputs to this gate. In order to analyze changes in frequency and power consumption, we will set 11 of these gates up in series to create a ring oscillator. Each LoOut (output from the inverter whose supply voltages have been shifted down) will be tied to the next gate’s PIN, which is tied to the gates of the PMOS transistors. This will result in the PMOS transistors being “overdriven” when the output of the previous gate is low, because a low output is less than ‘0’. Following the same logic, the HiOut output will be tied to NIN, the input which is tied to the NMOS transistors. Again, this will “overdrive” the NMOS’ when the output from the previous gate is high.



**Figure 2: 11-Gate Ring Oscillator Test Bench**

Figure 2 shows the test bench for the 11-gate ring oscillator proposed earlier in this section. Note that there are four supply voltages, one for VDD+, VDD-, VSS+, and VSS- (refer to Figure 1 for clarification of these pins). Changing the bias voltage will both shift VDD+ & VSS+ up and shift VDD- & VSS- down. Figure 3 shows a simulation to determine if adjusting the bias voltage does indeed have an impact on the frequency of this ring oscillator.



**Figure 3: Transient Response of Ring Oscillator**

The bottom two waveforms illustrate the response of the ring oscillator in Figure two when the bias voltage is zero. The top two waveforms are the responses when the bias voltage is 100 mV; the topmost response is at a high output pin, and the response directly below that is at a low output pin. Notice that, although the outputs swing between different ranges, the difference in the top and bottom of said ranges is still 1.1 V. It can be concluded from this simulation that adjusting the bias voltage does indeed affect the frequency of a ring oscillator.

**Figure 4: Frequency (Hz) of Ring Oscillator Vs. Supply Bias Voltage (V)**

Figure 4 shows how the frequency of the ring oscillator in Figure 2 changes as the bias voltage changes. The nominal voltage in these simulations was 1.1 V. The frequency increased by about 13% for a bias voltage of 100 mV compared to no bias. The power consumption vs. bias voltage is illustrated in Figure 5.

**Figure 5: Power Consumed (Watts) Vs. Supply Bias Voltage (V)**

As expected, the power consumption increased exponentially with an increase in the bias voltage. An important take-away from this analysis is that the power consumed by the ring oscillator can be reduced by applying a negative bias.

**Expected Outcomes**

As expected, our new two-inverter gate exhibits a change in frequency and power when the supply voltages are altered. Upon further analysis, we expect to find that the dynamic power of this circuit is greater than that of an equivalent inverter which has been body-biased. This is because the P and N inputs to each gate in the ring oscillator may not come at the same time due to the shifted supply voltages, resulting in some amount of short circuit power. This will be evaluated further in subsequent simulations.

Recall that the motivation for this project is to find a substitute for body-biasing effects in a FinFET, which is relatively unresponsive to body effects. Therefore, it is our goal to prove that our method of adjusting the supply voltages effectively increases the frequency and/or decreases the power consumption in a ring oscillator (and other applications), and not necessarily to prove that this is a better alternative to body biasing in MOSFETS which are susceptible to body effects.

**Timeline**

10/8/13 – First design review completed

* Frequency analysis to determine if supply biasing is an effective way to make a circuit faster.
* Power analysis to compare supply biasing to body biasing to ensure that any increase in frequency would not result in a significant sacrifice in power, and vice versa.

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* Quantitative frequency and power analyses vs. supply bias.

10/17/13 – 11/12/13 – Explore leakage and short circuit currents

* Quantify leakage and short circuit currents in a ring oscillator made up of 11 of our 2-inverter gates.
* Explore ways to mitigate short circuit and leakage current.
* Design review II completed by 11/12/13

11/12/13 – 12/03/13 – Explore applications of the 2-inverter supply biased gate

* This may include applications in both traditional MOSFETs and FinFETs.
* Fabricate a ring oscillator as discussed above and test its response to supply biasing against our simulations.
* Final design review completed 12/03/13.

**References**

1. Tschanz, JW, JT Kao, SG Narendra, R Nair, DA Antoniadis, AP Chandrakasan, and V De. "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variation on microprocessor frequency and leakage." Solid-State Circuits, IEEE Journal of, n.d. 14 September 2013.

2. Tschanz, JW, S Narendra, R Nair, and V De. "Effectiveness of Adaptive Supply Voltage and Body bias for Reducing Impact of Parameter Variations in Low Power and High Performance Microprocessors." . Solid-State Circuits, IEEE Journal of, n.d. 21 September 2013.

3. Park, T, S Choi, DH Lee, and JR Yoo. "Fabrication of Body-Tied FinFETs (Omega MOSFETs) Using Bulk Si Wafers." . VLSI Technology, 2003. Digest of Technical Papers, n.d. 7 Oct 2013.